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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/730,832 | 12/08/2003 | Chong Ki Kwon | 5882P067 | 7570 |

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| EXAMINER | |
|---|---|
| NGUYEN, KHANH V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2817 | |

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/730,832 | KWON ET AL. | |
| | Examiner | Art Unit | |
| | Khanh V. Nguyen | 2817 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 3-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-7* is/are rejected.

7)☒ Claim(s) *3 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1, 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siniscalchi (6,522,200), cited in PTO-892 mailed on July 7, 2005.

Siniscalchi discloses the claimed invention except the voltage-current converter including first and second NMOS transistors. Siniscalchi (Fig. 4) discloses an amplifier circuit comprising: transistors (M11, M12), resistor (R), and current sources (404, 406) together can be configured as a voltage-current converter for converting voltages of a wide input range into currents, wherein transistors (M11, M12) are connected between power supply (VDD) and first and second output terminals via sources of transistors (M3-M6); transistors (M3-M6) can be configured as a current shared circuit for receiving the currents from the voltage-current converter and controlling output currents values depending on first and second control voltages (Vc +/-) to the respective gates of transistors (M3-M6); and transistors (M7-M10) and current source (not label) together can be configured as a current-voltage converter for converting the output currents from the current shared circuit into differential voltages (Out+, Out-) depending on bias voltage (Vb1/Vb2) in order to obtain a variable gain. Note, the reference circuit discloses transistors (M11, M12) are PMOS transistors and not NMOS transistors as claimed,

However, utilizing NMOS/PMOS is considered reversal of parts which involves only routine skill in the art. Furthermore, both types MOS transistors are very well known in the art and readily available. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ either transistors in the device of Siniscalchi without departing from the spirit of the invention.

Regarding claim 4, Siniscalchi discloses the claimed invention except the current shared circuit including NMOS transistors. Siniscalchi discloses a current share circuit including PMOS transistors (M3-M6) having the connections thereof and not NMOS transistors as claimed. However, utilizing NMOS/PMOS is considered reversal of parts which involves only routine skill in the art. Furthermore, both types MOS transistors are very well known in the art and readily available. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ either transistors in the device of Siniscalchi without departing from the spirit of the invention.

Regarding claim 5, Siniscalchi discloses the claimed invention except the claimed first and second resistors. Siniscalchi discloses transistors (M9, M10) can be read as first and second NMOS transistors driven by bias voltage (Vb2) and NMOS transistors (M7, M8) can be read as first and second current sources; and current sources (not label) which is well known in the art and can be replaced with a respective resistors which can be read as first and second resistors/loads.

Regarding claims 6, 7, Siniscalchi discloses transistors (M9, M10) can be read as first and second NMOS transistors driven by bias voltage (Vb2) and NMOS transistors (M7, M8) can be read as first and second current sources or third and fourth NMOS

transistors driven by bias voltage (Vb1); and current sources (not label) which is well known in the art and can be replaced with a respective resistors which can be read as first and second resistors/loads.

### *Allowable Subject Matter*

Claims 3, 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 3 calls for, among others, the voltage-current converter further comprises first and second current sources having the connections as claimed.

Claim 8 calls for, among others, each load comprises a PMOS, a NMOS, and a capacitor and current source.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh V. Nguyen whose telephone number is (571) 272-1767. The examiner can normally be reached from 8:00 AM - 3:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**KHANH VAN NGUYEN**
**PRIMARY EXAMINER**
**Art Unit: 2817**